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TSMC99-656

December 14, 2000

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 09/689,930 10/13/00
Chung-Shi Liu, Chih-Cheng Lin
NEW DUAL DAMASCENE PROCESS
Grp. Art Unit: 1756

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,877,076 to Dai, "Opposed Two-Layered Photoresist Process for Dual Damascene Patterning", teaches a dual damascene photo process using two photoresist layers with opposite types, one positive and one negative, photo sensitivities and a two-step exposure.

U.S. Patent 5,877,075 to Dai et al., "Dual Damascene Process Using Single Photoresist Process", describes a dual damascene process using a silylation process with a single photoresist process and a two-step exposure.

U.S. Patent 5,882,996 to Dai, "Method of Self-Aligned Dual Damascene Patterning Using Developer Soluble ARC Interstitial Layer", describes a method for patterning dual damascene interconnections in semiconductor chips through the use of a developer sobuble ARC interstitial layer.

U.S. Patent 5,906,911 to Cote, "Process of Forming a Dual Damascene Structure in a Single Photoresist Film", describes a dual damascene process using just one single layer of photoresist with two photomasks and selective silylation.

U.S. Patent 5,936,707 to Nguyen et al., "Multi-Level Reticle System and Method for Forming Multi-Level Resist Profiles", teaches a dual damascene photo process using single photoresist process.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761